ADVANCES ON LVRT IMPLEMENTATION AT LV NETWORKS IN THE PROSPECT OF MASS PENETRATION OF DERS

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ABSTRACT

This paper summarizes the recent advances on Low Voltage Ride Through (LVRT) implementation at Low Voltage (LV) networks, in the prospect of mass penetration of Distributed Energy Resources (DERs). The reported advances are the outcomes of DGRES-Pro project, focusing on the transformation of typical LV feeders into contemporary flexible electric apparatus, with the use of power electronics conversion unitsthat will able to accommodate mass penetration of DERs in a safe and effective manner.

Keywords – Low Voltage Ride Through; Distributed Energy Resouces; Power Electronics; Distribution Networks

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I. INTRODUCTION

The mass integration of Distributed Energy Resources (DERs) into distribution networks has necessitated the adoption of Low Voltage Ride Through (LVRT) requirements by relevant distribution networks codes over the last years [1]. LVRT is defined as the capability of generation units to remain connected to the electricity network (Transmission or Distribution level) during faults, providing voltage support, for a time duration that depends on the voltage drop at the point of common coupling (PCC). This distribution network transformation requires smart and flexible power electronic conversion units to implement all the operation/protection principles that LVRT scheme suggests.

In this context, a research project has been successfully conducted by the authors, namely “Application of advanced power electronic systems for the implementation of innovative protection schemes at LV distribution networks, in the prospect of mass penetration of DERs (DGRES-Pro)”. The project is funded by the Operational Program “Human Resources Development, Education and Lifelong Learning” and is co-financed by the European Union (European Social Fund) and Greek national funds.

In order to highlight the main aspects of the alterations that mass DER penetration and LVRT implementation bring on the operation of LV networks. the project had the following main research activities:

- Investigation of the adaptation of line protection means to LVRT requirements in LV distribution feeders with photovoltaic generators (PVs) [2].
- Study on harmonic injection anti-islanding techniques under the operation of multiple DER-inverters [3].
- Study on the loss of neutral in low voltage electrical installations with connected DERs – consequences and solutions [4].

In the following section, a summary of the outcomes of DGRES-Pro project is presented.

II. SUMMARY OF RECENT ADVANCES ON LVRT IMPLEMENTATION AT LV NETWORKS, IN THE PROSPECT OF MASS PENETRATION OF DERS

A. Investigation of the adaptation of line protection means to LVRT requirements in LV distribution feeders with PVs

In LV distribution feeders with DG units, a major challenge to meet LVRT requirements is the coordination with the feeder protection means. Typically, LV distribution feeders are protected by a fuse, which implements a non-settable time-overcurrent characteristic curve. As such, the fuse cannot be reconfigured after its installation, failing to meet line protection and DG LVRT requirements at the same time.

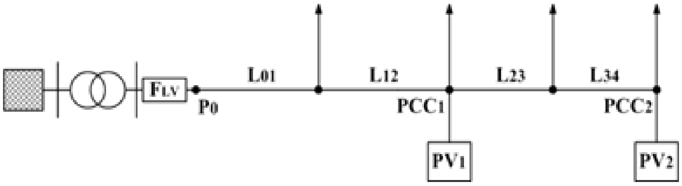

Figure 1. TEST DISTRIBUTION FEEDER.

This issue is examined with the aid of Fig. 1, which depicts a typical 50 Hz; 0.4 kV;, LV distribution feeder which is modeled with DIgSILENT Power Factory; all the segments of this feeder consist of 150-mm2 NAYY cable. Segments L01 and L12 are 25-m long, whereas segments L23 and L34 are 20-m long. The external grid is represented by an equivalent source with a maximum short-circuit power of 200 MVA at 20 kV. The feeder departs from a 20/0.4 kV transformer. The total system load is 140 kVA (133 kW). Finally, two 20 kW PV units are considered connected to points PCC1 and PCC2,PV1 and PV2, respectively (the simulation is based solely on PV units, being the predominant DER-units in LVRT networks). It is noted that the maximum steady-state short-circuit contribution of each PV-unit is limited to its nominal load current. Also note that PV1 and PV2 units operate according to the LVRT scheme of [5].

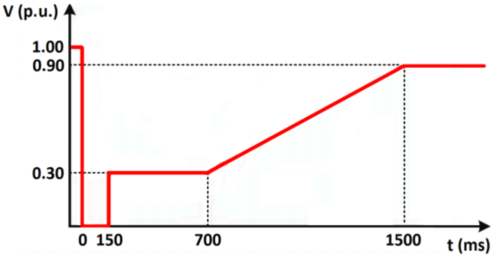

FIGURE 2. ADOPTED LVRT CHARACTERISTIC

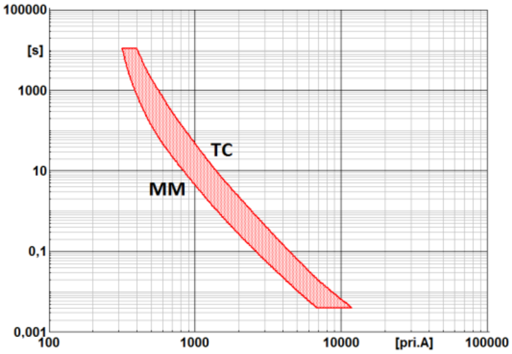

FIGURE 3. TIME-OVERCURRENT CHARACTERISTIC OF FUSE F_{LV}.

This LVRT characteristic is shown in Fig. 2, where a common 250 A gL fuse (FLV in Fig. 1) is installed for the feeder protection; fuse current rating is selected according to the maximum load current in the examined feeder. Fig. 3 illustrates both the minimum-melting (MM) and the total-clearing (TC) time-overcurrent characteristics of fuse FLV. Considering the case of a short-circuit occurs at the above line, the LVRT operation of PV-units might be interrupted by the fuse, leading the system into an islanding operation [6]-[9].

In order to better demonstrate the above-described problem, fault-simulations have been performed for all common fault types: line-line-line (LLL), double-line (LL), double-line-ground (LLG), and single-line-ground (SLG). According to the results in Table I, in all the examined fault-cases, LVRT requirements are violated, since fuse F_{LV} melts (or even starts melting) before the required time duration of PV-connection expires. These indicative results highlight the potential conflict of line protection (fuse) and LVRT requirements in LV networks.

TABLE I. INDICATIVE SIMULATION RESULTS

		t_{MM}/t_{TC} (in ms) of F_{LV} in each fault-case		
Fault position		**P_0**	**PCC_1**	**PCC_2**
Fault type	**LLL**	7/41	13/79	21/133
	LL	11/65	20/128	32/216
	LLG	7/40	12/76	21/138
	SLG	7/40	22/144	50/357

In order to avoid reconsideration of the LV distribution networks protection, a solution to the above problem would be the limitation of the short-circuit current that flows through the LV fuse, so as for the latter to be suitably delayed, allowing the PV-units to stay connected for the time intervals that LVRT requirements impose. In the frame of DGRES-Pro project, a power electronic-based current-limiting device (CLD) solution has been developed, presented in Fig. 4, to limit the short-circuit current that flows through the LV fuse. The control diagram of the proposed CLD is depicted in Fig. 4 and implements a dual current-limiting approach (fixed or adaptive); $i_A(t)$ and $v_{P0}(t)$ represent the instant values of current and voltage at fuse location P_0, respectively, . The CLD device therefore resables a controllable impedance, placed in series with the fuse, as in Fig. 4.

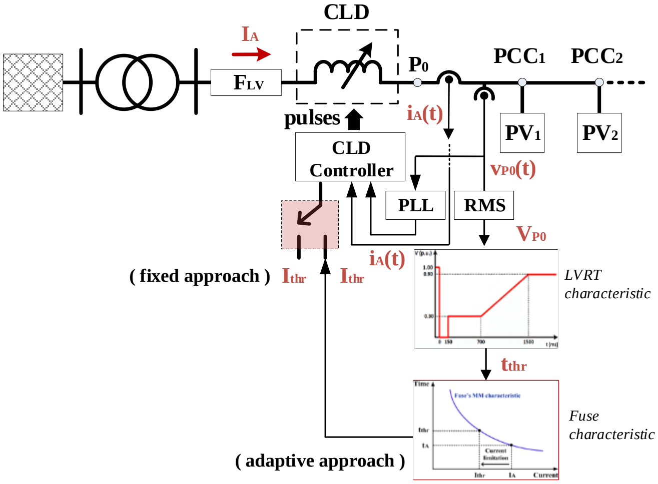

FIGURE 4. THE PROPOSED SOLUTION FOR FLEXIBLE (POWER ELECTRONIC-BASED) FAULT CURRENT LIMITATION.

In terms of hardware (power electronics) implementation, CLD is an ac-chopper which regulates the fundamental current component. Many topologies can be utilized to implement the ac-chopper. A particularly appealing topology though is the one proposed in [10]. Nevertheless, regardless the chosen topology, the design should meet the following two requirements:

a) The efficiency of CLD should be as high as 98%.
b) The power density of CLD should match current density of power grid-tied inverters (> 5 kW/kg).

Modern wind bandgap semiconductors (such as Silicon Carbide-SiC and Gallium Nitride-GaN) constitute an excellent solution to meet the above requirements.

B. Study on harmonic injection anti-islanding techniques under the operation of multiple DER-inverters

Apart from the LVRT scheme implementation at LV distribution networks, an additional critical issue that raises from the mass penetration of DERs is the effective anti-islanding protection. Although anti-islanding protection is well established in grid-tied PV inverters, all commercial solutions are designed for inverter sole operation [3]; thus, the effectiveness of commercial anti-islanding protection schemes in case of parallel inverters operation at the same PCC is poorly investigated [6], [9].

In this context, our work in the frame of DGRES-Pro project has also taken into consideration the impact of mass penetration of DERs on anti-islanding protection schemes. Our main focus was on harmonic injection-based techniques, because they are referenced in literature as an appealing solution for anti-islanding protection of interconnected DER-systems [7], [8]. Those schemes do not disturb the output active-power of grid-tied inverter, they have reduced NDZ and provide fast island detection [7], [8]. Moreover, those schemes are highly dedicated to implementation in both high penetration levels of DERs and weak grid conditions, being the main theme of this work. According to those schemes, anti-islanding detection is based on the injection of selected harmonic current components and the evaluation of grid-response, typically through the comparison with a predefined threshold value.

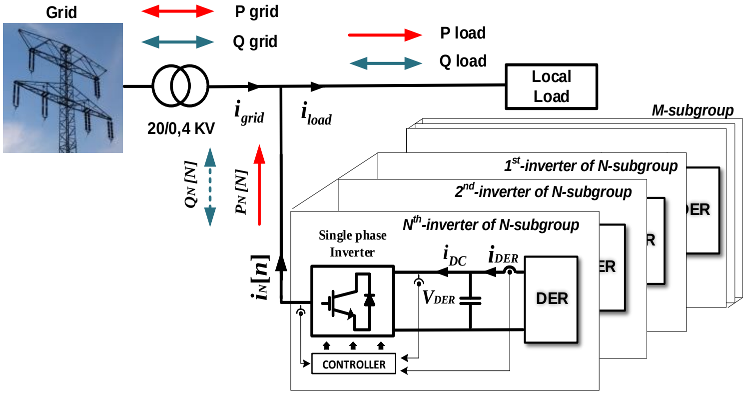

FIGURE 5. GENERAL DESCRIPTION OF THE SYSTEM UNDER STUDY.

The general description of multiple DRES-inverters connected at the same PCC is illustrated in Fig. 5. It consists of a subgroup of N-inverters that utilize a harmonic injection scheme, a subgroup of M-inverters (connected to the same PCC) that may or may not utilize an anti-islanding scheme, the local load, and the LV utility grid [9]. The power flow of each subsystem is also depicted in Fig. 5.

Considering the general system in Fig. 5, in the frame of this research activity, we proposed an advanced harmonic injection-based anti-islanding protection algorithm, illustrated in Fig. 6; the main idea is the introduction of an external integrator to cumulate the harmonic voltage components that have been induced by each inverter [9]. As such, the cumulative integral index will consider the individual impact of each inverter. It should be noted that a reset has to be performed periodically in this case, based on the periodicity of the harmonic injection of each inverter [9]. Consequently, the harmonic injection periodicity of each inverter (T_{rst} in Fig. 6) must be acknowledged beforehand, and be the same for all inverters, which is the main requirement of our proposed solution. Furthermore, the order of the harmonic injection should be an integer number, whereas the harmonic injection should be activated with respect to an agreed time-delay of PCC voltage; thus, the injected current components will not cancel each other. The time-delay could be agreed among the inverter manufacturers and included in the relevant prototyping standards.

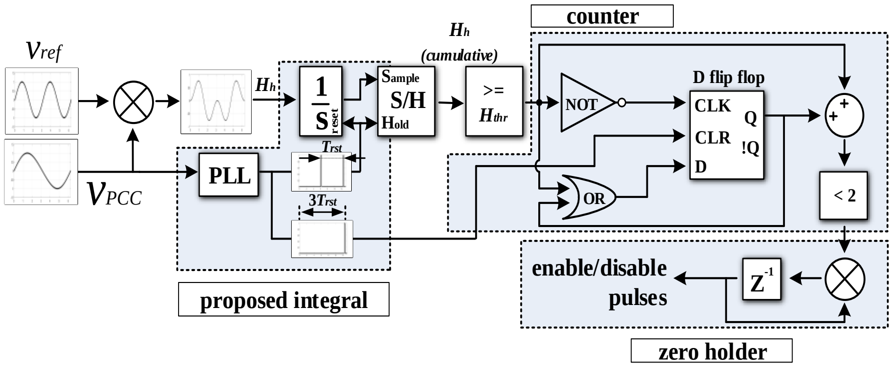

FIGURE 6. PROPOSED ANTI-ISLANDING SOLUTION IN THE PROSPECT OF MASS PENETRATION OF DERS AT LV NETWORKS.

The operation of the proposed (cumulative) technique is presented in Fig. 7. The case of two inverters has been considered, supporting the effectiveness of our solution.

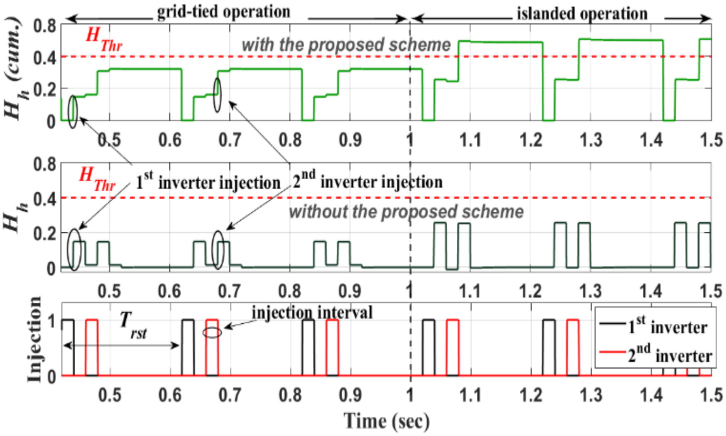

FIGURE 7. DEMONSTRATION OF THE PROPOSED SOLUTION (GRID-TIED AND ISLANDED OPERATION).

C. *Study on the loss of neutral in low voltage electrical installations with connected DERs – consequences and solutions*

Another critical issue that raises from the mass penetration of DERs at LV networks (i.e. building DER installations) is the loss of neutral conductor, which is directly related to the safety of both human life and the electrical installation. The interruption of neutral conductor is a known issue in distribution networks, yet not fully addressed in view of the forthcoming massive installation of DERs and storage units (including Vehicle-to-Grid concept). Such a condition may result in serious repercussions for the connected electrical installations and consumers. The consequences of neutral conductor loss depend mainly on the load balance conditions in a three-phase system, but also on the type of earthing system used and the location of neutral interruption (relatively to the load). Worst-case scenarios may include both damages to connected loads (due to overvoltages on single-phase circuits) and the creation of hazardous touch voltages on exposed conductive parts [11-13].

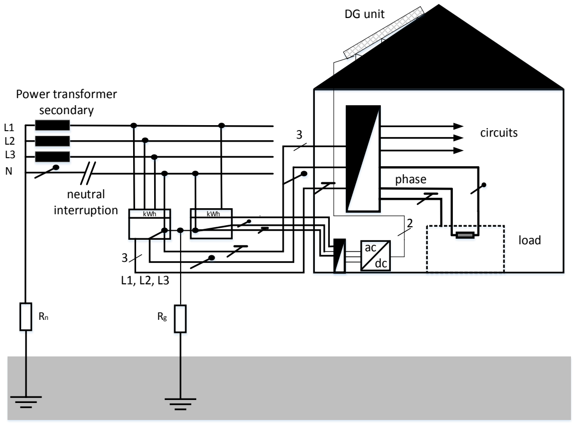

FIGURE 8. SYSTEM UNDER EXAMINATION.

In the frame of DGRES-Pro project, the loss of neutral conductor under mass penetration of DERs has been thoroughly investigated; Fig. 8 presents the considered typical electrical building installation understudy, employing TN grounding system. A four-pole cable inserts to the energy meter of the building installation, where the neutral is connected to the grounding system of the installation to be protected. All the exposed-conductive-parts of the installation are connected to the protective earth conductor (PE). In addition, a DER (i.e. a PV system, namely DG-unit) is installed on the rooftop of the building, injecting the generated electrical energy to the network.

As an initial step, a sensitivity analysis for the developed voltages on the protective conductor is carried out, considering the following parameters:

- the generated electric power by the DG-unit (5A, 10A, 15A)
- the local load (1kW, 4kW, 6kW)
- the grounding resistance of the installation (1Ω, 2Ω, 5Ω, 10Ω, 15Ω, 20Ω).

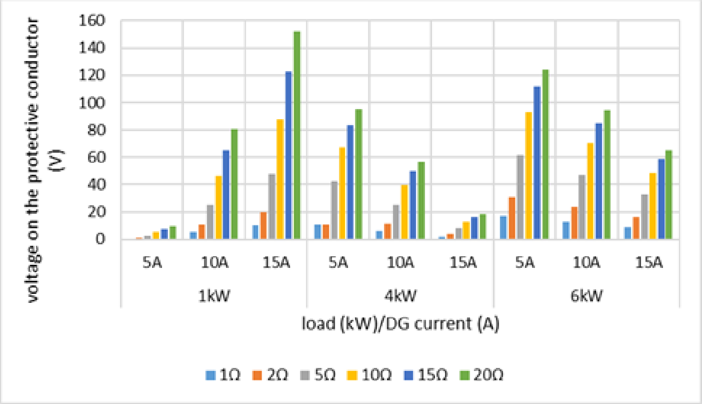

FIGURE 9. DEVELOPED VOLTAGES ON THE PROTECTIVE CONDUCTOR IN THE CASE WHERE A DG UNIT (A) IS NOT INSTALLED, (B) IS INSTALLED.

Fig. 9 depicts the obtained results in the case that a DER is installed; in this case, the power coming from the DER and the absorbed power by the load, are key factors that influence the developed potential on the protective conductor. If the injected (by the DER) and the absorbed (by the load) energy are almost equal, then the developed voltage on the protective conductor does not exceed the safety limit of 50V (see load 1kW, DER-unit current 5A and load 4kW, DER-unit current 15A) for all the grounding resistance values. It is worth mentioning that even for low grounding resistance values the developed voltages can exceed the safety limit, due to the difference between the generated and the absorbed energy (see load power 1kW, DG unit current 15A, grounding resistance 10Ω).

The proposed loss of neutral conduction method (in the frame of DGRES-Pro project) is depicted in Figs 10, 11. The proposed neutral conductor loss detection scheme is based on the estimation of both zero-sequence impedance $z_{0,rms,50Hz}$ and voltage $v_{0,rms,50Hz}$ at the fundamental frequency of 50 Hz. The measuring point of the line to neutral voltages, v_{abc}, and neutral current, i_n, is indicated in Figure 10. The zero-sequence voltage is calculated by summing the three-line to neutral voltages, as it is depicted in Fig. 11.

As Fig. 11 depicts, $z_{0,rms,50Hz}$ is compared with a predetermined threshold value $z_{0,thr}$ and if $z_{0,rms,50Hz} \geq z_{0,thr}$ then a neutral conductor interruption fault is indicated. It is noted that the impedance estimation method is not solely based on this proposed scheme, due to the incorrectly calculated values that arise under very high values of $z_{0,rms,50Hz}$ (in cases that $i_n \to 0$). For this reason, the impedance estimation scheme is activated only when the current of the neutral wire is above a threshold value, $i_{n,thr}$ (Switch1 at position 2). An overvoltage protection scheme operates complementary with the impedance estimation scheme and it is activated when the zero-sequence voltage is above the limit of 50V. This ensures the protection against hazardous touch voltages on exposed conductive parts.

Fig. 12 illustrates the loss of neutral conductor detection with the aid of the proposed methodology, considering the system in Fig. 10 with the technical characteristics of Table II (simulation results). The initialization time of the system is determined at 0.45s in order for the PV-Inverter to reach its nominal power value. When the neutral conductor interruption occurs a notable arise of the zero-sequence voltage $v_{0,rms,50Hz}$ emerges, while neutral current drops. The proposed scheme detects the fault by accurately estimating the grounding resistance value ($z_{0,rms,50Hz} = R_n+R_g = 10\ \Omega$, in Fig. 12).

TABLE II. SYSTEM TECHNICAL PARAMETERS

$\mathbf{P_{pv\text{-}inv}}$	4 kW
$\mathbf{P_{Load}}$	6 kW
$\mathbf{z_{tr}}$	0.001 + j1e-6 Ω
$\mathbf{R_n}$	1 Ω
$\mathbf{R_g}$	9 Ω
$\mathbf{V_{abc}}$	230 V_{rms} (line to neutral)
$\mathbf{t_{disc}}$	0.5 s
$\mathbf{i_{n,thr}}$	0.5 A
$\mathbf{z_{0,thr}}$	5 Ω

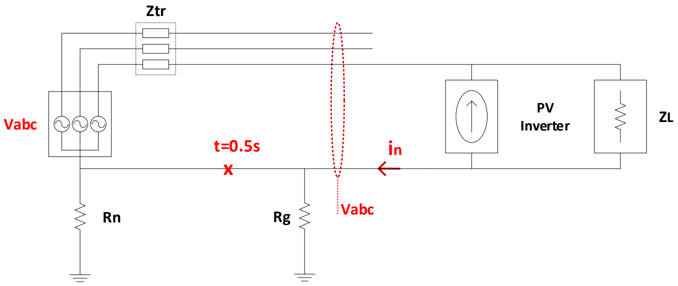

FIGURE 10. EQUIVALENT SYSTEM MODEL.

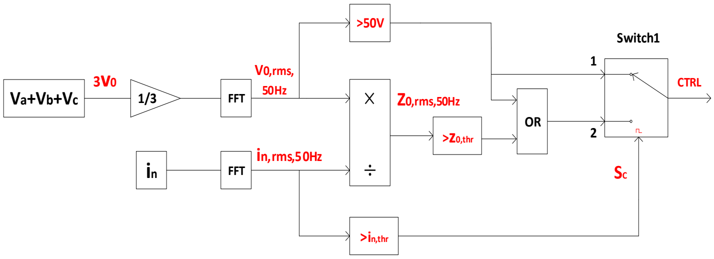

FIGURE 11. PROPOSED LOSS OF NEUTRAL CONDUCTOR DETECTION SCHEME.

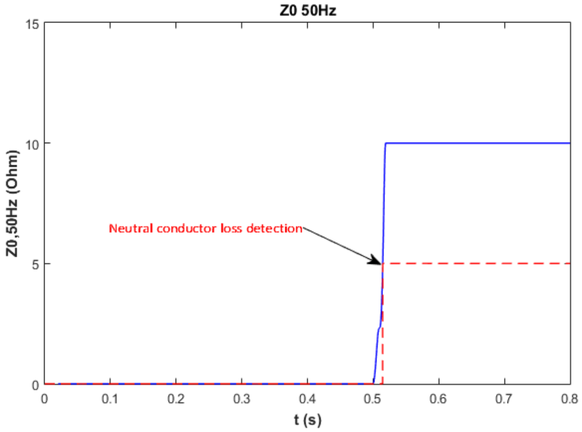

FIGURE 12. LOSS OF NEUTRAL CONDUCTOR DETECTION ACCORDING TO THE PROPOSED METHODOLOGY.

III. CONCLUSIONS

This paper summarizes the recent advances on LVRT implementation at LV networks, in the prospect of mass penetration of DERs, in the frame of DGRES-Pro project. The main research activities of this project regarded a) the investigation of the adaptation of line protection means to LVRT requirements in LV distribution feeders with photovoltaic generators (PVs), b) the study on harmonic injection anti-islanding techniques under the operation of multiple DER-inverters, and c) the study on loss of neutral in low voltage electrical installations with connected DERs – consequences and solutions. All these research activities have concluded to successful technological solutions that contribute to the main goal of transforming the typical LV feeders into contemporary flexible electric apparatus, by means of power electronics conversion units, able to accommodate mass penetration of DERs in a safe and effective manner.

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